



# **AMD-760™ MP Chipset Overview**

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## Revision History

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<b>Date</b>	<b>Revision</b>	<b>Description</b>
C	October 2001	Second Edition Public Release. - Add Athlon MP references and text to facilitate the Athlon MP launch.
B	May 2001	Initial Public Release.
A-1	May 2001	Initial NDA Release.

## Overview

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The AMD-760™ MP chipset is a high performance two-way multiprocessor core logic solution for the Athlon™ MP class processors. The high-performance of the chipset is attributed to an enhanced AMD Athlon™ system bus, support for DDR (Double Data Rate) memory technology, and AGP-4X Graphics Interface. Together with other sophisticated core logic in memory and I/O control, system and power management, the AMD-760MP chipset provides a powerful solution for server and workstation platforms.

The AMD-760MP chipset consists of the following components.

- AMD-762™ system controller (Northbridge)
- AMD-766™ peripheral bus controller (Southbridge).

Key features of the chipset are as follows:

- Dual point-to-point, high-speed 266MHz<sup>1</sup> AMD system buses (supporting up to two processors)
- PC2100<sup>2</sup> DDR (Double Data Rate) memory subsystem (supporting up to 4 GB of memory space)
- AGP-4X Graphics Interface (supports 1X and 2X modes)
- PCI 2.2 Compliant 33 MHz – 32/64-bit PCI Bus Interface
- Two-channel EIDE Interface supporting ATA 33/66/100 modes
- LPC bus
- Flash memory/GPIO Interface
- USB 1.1 Compliant OHCI host controller supporting four ports
- SM-Bus
- IOAPIC support
- Serial IRQ support
- Power management support

These features combine to deliver unprecedented performance to platforms implementing AMD processor technology.

Figure 1 shows the system architecture of the AMD-760 MP chipset.

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<sup>1</sup> The 266 MHz speed represents a 133 MHz Clock signal, with data transfers on both clock edges. This produces a (133 MHz clock) x (2 data transfers/clock) = 266M transfers/sec = 266-MHz data rate.

<sup>2</sup> PC2100 represents DDR memory DIMMS that provide data rates of 2100 MB/s, calculated as (133-MHz clock) x (2 data transfers/clock) x (8 Bytes/transfer) ≈ 2100 MB/s.

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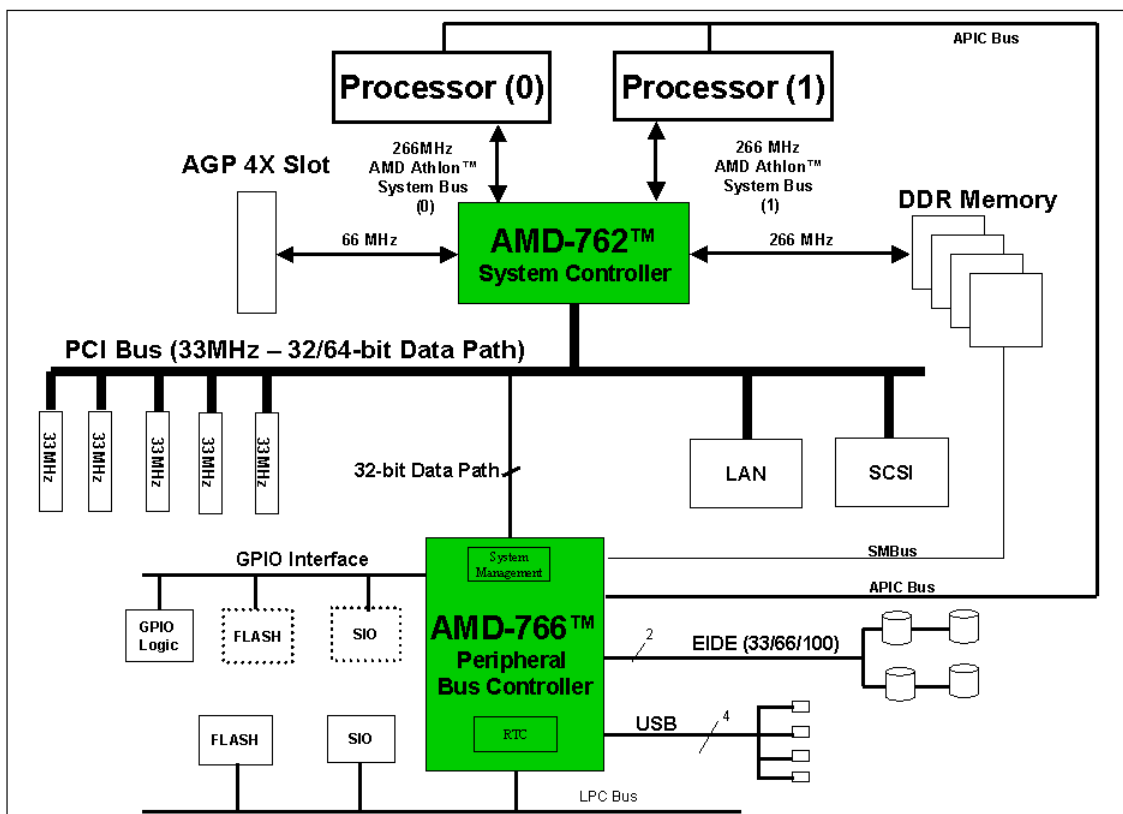


Figure 1. AMD-760™ MP Chipset High-Level System Architecture

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## AMD-762™ System Controller

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The AMD-762™ System Controller provides the bridging function between the high-speed host-processor buses, AGP Graphics subsystem, DDR memory subsystem, and the PCI interface.

Key features of the AMD-762 system controller are as follows:

- Two 266 MHz point-to-point AMD system buses, providing uni-processor or 2-way Symmetric Multiprocessor capability
- PC2100 DDR (Double Data Rate) Memory Controller with support for up to 4 GB of memory space (supports four Registered DIMM slots)
- AGP-4X Interface (supporting 1X and 2X modes)
- Dual Mode PCI 2.2 Compliant PCI Bus Interface
  - 33 MHz clock with 32-bit and 64-bit data path support. (Supports up to seven PCI devices<sup>3</sup>)
  - 66 MHz clock with 32-bit and 64-bit data path support. (Supports up to two PCI slots)
- A 949-pin Ceramic Column Grid Array (CCGA) package
- 2.5 V Core

The AMD-762 system controller also supports the 66 MHz/32-bit/64-bit PCI bus mode<sup>4</sup>. In this mode, the AMD-762 system controller supports only two 66-MHz PCI bus slots. For designs requiring both 66 MHz and 33 MHz PCI capability, compatible Southbridge components implementing PCI-to-PCI bridging can be used to provide 33 MHz bus expansion.

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<sup>3</sup> The AMD-762™ system controller provides eight PCI Bus REQ/GNT# signal pairs.

- One pair dedicated to the Southbridge (SBREQ, SBGNT#)
- 7 pairs dedicated to other PCI devices (REQ[6:0], GNT[6:0]#)

From a bus loading and signal integrity perspective, AMD designs and tests its AMD-762 system controller-based reference design platforms to accommodate five PCI bus slots (33-MHz mode). Neglecting the Southbridge, this configuration leaves two REQ/GNT# signal pairs available for additional motherboard PCI slots and devices (for example, SCSI components, Network Interface Components, etc). It is up to the system designer to perform the necessary analysis and testing to determine if additional slots and devices can be supported.

<sup>4</sup> This mode is not supported when the AMD-762 System Controller is used in conjunction with the AMD-766™ Peripheral Bus Controller. This mode can only be used when the Northbridge is interfaced to a PCI 66 MHz capable Southbridge that is compatible to the AMD-762 System Controller.

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## **AMD-766™ Peripheral Bus Controller**

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The AMD-766™ peripheral bus controller integrates the I/O subsystems — allowing communication to peripheral devices. Included in the AMD-766 peripheral bus controller are the following features:

- PCI 2.2 compliant 33 MHz/32-bit PCI Bus Interface
- LPC (Low Pin Count) bus interface
- GPIO/Flash Interface: 8 bits wide; support for Flash BIOS and attachment of General Purpose I/O Devices (for example, buttons and switches)
- Several internal resistors added for system cost reduction
- UDMA 33/66/100 compatible EIDE bus master controller
- Support for a primary and a secondary dual-drive port
- Supports PIO modes 1-4
- ATAPI
- Two separate FIFOs for DMA accesses and read prefetch and write buffers for PIO accesses.
- OHCI-based USB 1.1 host controller (Includes a root hub and support for four ports)
- Extensive ACPI-compliant power management logic
- Programmable C2, C3, and Power-On-Suspend, Suspend-to-RAM, Suspend to disk, and soft off states
- Throttling
- Hardware traps
- System inactivity timer
- System management logic, including Total Cost of Ownership (TCO) registers
- Privacy/security logic, including ROM access control
- 32 pins multiplexed with General Purpose IO (GPIO) functionality
- AT-compatible Interrupt Controller (8259-based)
- Programmable interval timer (8254-based)
- Real-Time Clock (RTC)
- 256 bytes of CMOS RAM
- Battery-powered
- ACPI-compliant extensions
- Register-compatible I/O APIC (82093)
- Legacy AT logic (including Port 61h logic, Gate A20 logic, Port 92h logic, etc)
- SMBus controller with one SMBus port
- A 272-pin BGA package
- 3.3-volt core and output drivers; 5-V tolerant input buffers